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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,120	07/31/2003	Gerard Chauvel	TI-35486 (1962-05420)	3950

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,120	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are pending.

2. The office acknowledges the following papers:

Foreign priority papers filed on 3/15/2004,

Drawings filed on 3/2/2004,

Drawings filed on 2/2/2004,

Oath filed on 12/18/2003,

Oath filed on 12/09/2003.

Priority

3. This application claims priority to provisional application 60/400,391. The effective filing date for those claims which have proper support in the provisional application is 7/31/2002.

Drawings

4. The Examiner contends that the drawings submitted on 3/2/2004 are acceptable for examination proceedings.

Specification

5. The disclosure is objected to because of the following informalities:

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A suggested title is "Multimode processor with coprocessor to execute unsupported instructions."

7. The section cross-reference to related applications contains many co-pending applications. However, the application numbers have been left out and need to be added. If any of the application numbers have become patents, then the patent number should be added instead.

8. On page 11, line 4 of the specification reads "that the control logic 210 is connected." This should be changed to "that the control logic 218 is connected."

9. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

10. Appropriate correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

12. Claims 1-6 are rejected under 35 U.S.C. §102(e) as being anticipated by Barry (U.S. 6,865,663).

13. As per claim 1:

Barry disclosed a system, comprising:

A first processor having fetch logic and decode logic, the first processor fetches instructions from memory using said fetch logic and decodes said instructions with said decode logic (Barry: Figure 11 element 1120, column 12 lines 55-67 continued to column 13 lines 1-16)(The coprocessor fetches the instructions and executes them.); and

A second processor coupled to said first processor, the second processor fetches an instruction from memory, loads said instruction in the decode logic of the first processor, thereby permitting the first processor to decode said instruction without using the fetch logic (Barry: Figure 11 element 1110, column 12 lines 55-67 continued to column 13 lines 1-16)(The control processor fetches instructions and places them in the COIN register of the coprocessor.).

14. As per claim 2:

Barry disclosed the system of claim 1 wherein said first processor includes a port, the port is coupled to the decode logic and addressable by the second processor (Barry: Figure 11 element 1123, column 13 lines 4-16)(The COIN register has the same functionality of a port.).

15. As per claim 3:

Barry disclosed the system of claim 2 wherein said loads said instruction in the

decode logic of the first processor comprises writing to a pre-determined address mapped to the port (Barry: Figure 11 element 1123, column 13 lines 4-16)(The COIN register has a specific address that's written to.).

16. As per claim 4:

Barry disclosed the system of claim 1 wherein the first processor switches between at least two modes of operation (Barry: Column 12 lines 55-67 continued to column 13 lines 1-16)(The first mode is the coprocessor fetching and executing instructions. The second mode is the control processor fetching and loading instructions into the COIN register for the coprocessor to execute.).

17. As per claim 5:

Barry disclosed the system of claim 4 wherein the first processor said fetches instructions from memory using said fetch logic and decodes said instructions with said decode logic in a first mode of said at least two modes of operation (Barry: Column 12 lines 55-67 continued to column 13 lines 1-16)(The first mode is the coprocessor fetching and executing instructions. The second mode is the control processor fetching and loading instructions into the COIN register for the coprocessor to execute.).

18. As per claim 6:

The system of claim 4 wherein the second processor said fetches an instruction from memory, loads said instruction in the decode logic of the first processor, thereby permitting the first processor to decode said instruction without using the fetch logic in a second mode of said at least two modes of operation (Barry: Column 12 lines 55-67 continued to column 13 lines 1-16)(The first mode is the coprocessor fetching and

executing instructions. The second mode is the control processor fetching and loading instructions into the COIN register for the coprocessor to execute.).

19. Claims 7-12 and 14-16 are rejected under 35 U.S.C. §102(e) as being anticipated by Park et al. (U.S. 6,832,305).

20. As per claim 7:

Park disclosed a method, comprising:

Fetching and decoding instructions in a first processor (Park: Figure 1 element 120, column 3 lines 26-37)(The coprocessor is the first processor and has fetch and decode abilities.);

Detecting an unsupported instruction that is not executable by the first processor (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder detects instructions that are executable by the CPU and not executable by the coprocessor. Thus having the same functionality.);

Executing said unsupported instruction in a second processor (Park: Figure 1 element 110, column 3 lines 26-37); and

Providing the first processor with a supported instruction that is executable in the first processor without the first processor fetching said instruction (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The CPU detects a coprocessor instruction by the predecoder, and sends it to the coprocessor without the coprocessor fetching the instruction. Thus having the same functionality.).

21. As per claim 8:

Park disclosed the method of claim 7 wherein providing the first processor with a supported instruction comprises loading the supported instruction in decode logic of the first processor (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The instruction is loaded into the decoder of the coprocessor through the coprocessor instruction register.).

22. As per claim 9:

Park disclosed the method of claim 7 further comprising detecting patterns of supported and unsupported instructions yet to be executed to determine when to perform said providing the first processor with a supported instruction that is executable in the first processor without the first processor fetching said instruction (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder detects a supported instruction of the coprocessor and sends it to the coprocessor without it fetching the instruction.).

23. As per claim 10:

Park disclosed the method of claim 9 wherein said patterns comprise an unsupported instruction followed by less then a threshold number of consecutive supported instruction before the next unsupported instruction (Park: Figure 1 element 113, column 4 lines 1-30).

24. As per claim 11:

Park disclosed a system, comprising:

A first processor having fetch logic and decode logic, the first processor fetches supported instructions from memory using said fetch logic and decodes said supported instructions with said decode logic (Park: Figure 1 element 120, column 3 lines 26-

37)(The coprocessor is the first processor and has fetch and decode abilities.);

A second processor, the second processor executes unsupported instructions (Park: Figure 1 element 110, column 3 lines 26-37);

Means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The CPU detects a coprocessor instruction by the predecoder, and sends it to the coprocessor without the coprocessor fetching the instruction. Thus having the same functionality.);

Means for coordinating when said loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction occurs (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The CPU detects a coprocessor instruction by the predecoder, and sends it to the coprocessor without the coprocessor fetching the instruction. Thus having the same functionality.).

25. As per claim 12:

Park disclosed the system of claim 11 wherein said means for loading a supported instruction in said decode logic of the first processor so than the first processor decodes but does not fetch the supported instruction comprises coupling the decode logic to a port addressable by the second processor, wherein the second processor fetches the supported instruction and loads said supported instruction in the decode logic of the first processor by accessing said port (Park: Figure 1 element 121, column 4 lines 31-48)(A port is an interface which data is transferred from one computer

to another. The register file allows data to be transferred from one processor to another. Thus having the same functionality.).

26. As per claim 14:

Park disclosed the system of claim 11 wherein said means for coordinating when said loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction occurs comprises a control program that examines patterns of supported and unsupported instructions yet to be executed and causes the first processor to switch between multiple instruction execution modes according to the patterns (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder detects a supported instruction of the coprocessor and sends it to the coprocessor without it fetching the instruction.), wherein said loading a supported instruction in the decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction is one of said multiple instruction execution modes (Park: Figure 1 element 121, column 4 lines 31-48)(The CPU sending instructions to the coprocessor is one mode of execution.)

27. As per claim 15:

Park disclosed the system of claim 14 wherein said control program runs on the second processor (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder is located on the CPU.).

28. As per claim 16:

Claim 16 essentially recites the same limitations of claim 10. Therefore, claim 16 is rejected for the same reasons as claim 10.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305).

31. As per claim 17:

Park disclosed the system of claim 16.

Park failed to teach wherein said threshold number is three.

However, it would have been obvious to one of ordinary skill in the art that the threshold number could be 3. By making the threshold 3, the coprocessor could disable fetching because it knows that instructions will be received from the CPU. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a threshold of 3 to avoid wasteful processing.

32. Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of Chaudhry et al. (U.S. 6,681,318).

33. As per claim 13:

Park disclosed the system of claim 12.

Park failed to teach wherein a switch permits said coupling the decode logic to the port addressable by the second processor.

However, Chaudhry disclosed wherein a switch permits said coupling the decode logic to the port addressable by the second processor (Chaudhry: Figure 1 element 110, column 4 lines 37-41)(The switch is coupled to two processors and indirectly coupled to the decode unit in each of the processors.).

An advantage of using a switch is that it can be turned off when it's not being used. This would be advantageous to Park's system of connecting data between the processors so that the bus line connecting the processors to transferring instructions could be turned off when it's not being used. One of ordinary skill in the art would have been motivated to use a switch between the processors to control data flow so that data isn't needlessly transferred between the processors. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a switch between the CPU and coprocessor of Park for the advantage of turning off the data flow between the two when it's not needed.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Li et al. (U.S. 6,230,278), taught a port and switch that can be changed to support multiple execution modes.

Capelli (U.S. 6,240,468), taught multiple processors with multiple modes of execution.

Agami et al. (U.S. 6,598,098), taught a port that can be changed to support multiple execution modes.

Goetz et al. (U.S. 5,854,913), taught multiple processors with multiple modes of execution to support two distinct ISA's.

Gorishek, IV et al. (U.S. 6,308,255), taught multiple processors running native and non-native code with one processor being able to send code to the other without it fetching the instruction.

Gorishek, IV et al. (U.S. 6,480,952), taught multiple processors running native and non-native code with one processor being able to send code to the other without it fetching the instruction.

Chung et al. (U.S. 6,950,929), taught multiple processors with a first processor sending an instruction it can't execute to the second processor, bypassing the fetch stage in the second processor.

Moyer et al. (U.S. 6,505,290), taught multiple processors with multiple modes of execution.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

RICHARD L. ELLIS
PRIMARY EXAMINER